

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

Paper No. 48

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte PHILIP A. BOUREKAS, AVIGDOR WILLENZ
AND YESHAYAHU MOR

Appeal No. 96-3244
Application 08/238,192¹

ON BRIEF

Before HAIRSTON, TORCZON, and CARMICHAEL, Administrative
Patent Judges.

HAIRSTON, Administrative Patent Judge.

¹ Application for patent filed May 4, 1994. According to applicants, the application is a continuation of Application 08/070,007, filed May 28, 1993, now abandoned; which is a continuation of Application 07/715,523, filed June 14, 1991, now abandoned.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1, 2, 4, 6 through 9, 11 and 13. In a first Amendment After Final (paper number 33), claim 8 was amended. Appellants' second Amendment After Final (paper number 39) was not entered by the examiner (paper number 40).

The disclosed invention relates to the testing of a circuit.

Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. In a logic circuit having a plurality of output control signals and a plurality of input/output signals, a reset circuit comprising:

a first input means for receiving a reset signal having an asserted state and a negated state;

a second input means for receiving a mode signal having an asserted and a negated state; and

a circuit, coupled to receive said reset signal and said mode signal, for generating a first control signal to force each of said output control signals to a negated state and a second control signal for causing said input/output signals to be tristated, such that (i) when said reset signal is in said asserted state and said mode signal is in said asserted state, said first control signal is asserted to force each of said output control signals to a negated state and said second control signal is asserted to tristate said input/output signals for as long as said mode signal is in said asserted state, (ii) when said mode signal transitions from said

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asserted state to said negated state while said reset signal remains in said asserted state, said first control signal is negated to no longer force any of said output signals [to] a negated state; and (iii) when said reset signal transitions from said asserted state to said negated state while said mode signal is in said asserted state, said second control signal is asserted to cause said input/output signals to remain tristated until said reset signal is again received in said asserted state.

The reference relied on by the examiner is:

Langone et al. (Langone)	4,743,842	May
10, 1988		

Claims 1, 2, 4, 6 through 9, 11 and 13 stand rejected under the first and second paragraphs of 35 U.S.C. § 112 for lack of enablement and for being indefinite.

Claims 1, 2, 4, 6 through 9, 11 and 13 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Langone.

Reference is made to the briefs² and the answers for the respective positions of the appellants and the examiner.

OPINION

All of the rejections are reversed.

A common thread woven throughout the rejections under 35 U.S.C. § 112 is the examiner's insistence that appellants

² Appellants' first and second Reply Briefs (paper numbers 42 and 44) were not entered by the examiner (paper numbers 43 and 45).

provide more details concerning the microprocessor disclosed in the specification, and that appellants directly claim a microprocessor. In response to the examiner's rejections, appellants argue (Supplemental Reply Brief (paper number 46), page 3) that the examiner is "looking in the wrong place" when he looks to appellants' specification, as opposed to claim 1, to determine what is appellants' invention. According to appellants, claim 1 "clearly recites that the invention is a reset circuit in a logic circuit" (Supplemental Reply Brief, page 3), and that "to enable making and using Appellants' invention, it is not essential to describe the microprocessor" (Supplemental Reply Brief, page 4) because "[a]ppellants' specification clearly teaches Appellants' claimed reset circuit on pages 5-8 and illustrates specific aspects of such a reset circuit in the figures" (Supplemental Reply Brief, pages 8 and 9). We agree. There is nothing indefinite about claim 1, and this claim is fully enabled by the disclosure. The same holds true for the other claims³ on appeal. The

³ In claim 8, the phrase "the step of providing a terminal used" is not clear, and in claim 9, the phrase "said disabling step" lacks antecedent basis.

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rejections of claims 1, 2, 4, 6 through 9, 11 and 13 under the first and second paragraphs of 35 U.S.C. § 112 are reversed.

The 35 U.S.C. § 102(b) rejection of claims 1, 2, 4, 6 through 9, 11 and 13 is reversed because the gate testing circuit disclosed by Langone does not disclose any of the reset circuit

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structure of claims 1, 2, 4 and 11 or any of the reset circuit
steps of claims 6 through 9 and 13.

DECISION

The decision of the examiner rejecting claims 1, 2, 4, 6
through 9, 11 and 13 under the first and second paragraphs of
35 U.S.C. § 112, and under 35 U.S.C. § 102(b) is reversed.

REVERSED

KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
)	
)	
)	BOARD OF PATENT
RICHARD TORCZON)	APPEALS AND
Administrative Patent Judge)	INTERFERENCES
)	
)	
JAMES T. CARMICHAEL)	
Administrative Patent Judge)	

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